REMARKS

Claims 1-16 stand examined in the instant application. Claims 12, 13, and 16 have been indicated by the Examiner to be allowable. Claims 1-11 are rejected and claims 14 and 15 have been objected to. These objections and rejections are addressed in the appropriate sections below. By virtue of this response, Claim 1 has been amended. Claims 17 – 19 have been added. Amendment and cancellation of certain claims are not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

In view of the preceding amendments and the remarks made herein, the present application is believed to be in condition for allowance.

Rejection of claims 1-7

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Application Publication No. 2003/0198077 to Ueda et al., under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,038,191 to Hasegawa et al., and under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0037106 to Lu et al. Applicants respectfully traverse these rejections to claim 1 as amended.

Applicants submit that Ueda, Hasegawa, and Lu have not disclosed the column address signal unit of the column decoder in their memory devices. The column address signal unit includes a word line connected to a row decoder for selecting the word line, a bit line connected to the column decoder for selecting the bit line, and a readout circuit connected to the column decoder to read memory data from the memory cell.

For at least the aforementioned reasons, it is respectfully submitted that the cited prior art references fail to disclose each and every element of claim 1. As a result, Applicants respectfully request that the rejection of claim 1 and its dependent claims 2-7 be withdrawn.

Rejection of claims 8-9

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Claims 8-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Application Publication No. 6,700,813 to Inui et al (hereinafter Inui). Applicants respectfully traverse these rejections.

Applicants submit that the Inui reference does not disclose at least the elements of "word lines for connecting the gates of said field-effect transistors in common in the row direction of said matrix," and "source drive lines for connecting the sources of said field-effect transistors in common in said row direction" of claim 8. The sources of the field effect type transistors of Inui are grounded (see Inui Figure 1, element T11, etc.) whereas sources of the field effect type transistors of the present application are connected to source drive lines (see Figure 2 of present application). In addition, according to Inui, the gates of the field effect type transistors are connected to a memory cell selection line (see Inui Figure 1, element SL1, etc.) while gates of the field effect type transistors of the present application are connected to word lines (see Figure 2 of present application). Thus, Inui does not anticipate each and every element of claim 8 and its dependent claim 9.

Rejection of claims 10-11

Claims 10-11 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0037106 to Lu et al (hereinafter Lu). Applicants respectfully traverse these rejections.

Applicants submit that Lu does not disclose features of claim 10 of the present invention, namely, "word lines for connecting the anodes of said diodes in common in the row direction of said matrix, and bit lines for connecting one terminal of each of said variable resistors in common in the column direction of said matrix, wherein the cathodes of said diodes are connected to the other terminals of said variable resistors." However, according to Figure 2 of Lu, anodes of diodes 214 are connected to one end of variable resistors 216, the other end of the variable resistors 216 are connected to word lines 126 disposed in the horizontal direction of the matrix, and cathodes of the

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diodes 214 are connected to bit lines 118 disposed in the vertical direction of the matrix. Therefore, Lu does not anticipate each and every element of claim 10 and its dependent claim 11.

Objection of claims 14 and 15

For the reasons presented above, since claims 8-9, which claim 14 is dependent from, are not anticipated by Inui, claim 14 is allowable in its original form. Similarly, since claims 10-11, which claim 15 is dependent from, are not anticipated by Lu, claim 15 is allowable in its original form.

Support for claims 1, 17 - 19

The support for claims 1 and 17-19 is found in figures 3, 5, 7, and their corresponding descriptions.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 544782000200. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: July 11, 2005

Respectfully submitted,

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